An Analytic Method to Determine GaAs FET Parasitic Inductances and Drain Resistance Under Active Bias Conditions

Charles F. Campbell, *Member, IEEE,* and Steven A. Brown, *Member, IEEE*

***Abstract*—An analytic technique to determine the parasitic inductances, source resistance, and drain resistance of the FET equivalent circuit is presented in this paper. The method exploits the frequency dependence of the extracted circuit parameters to determine the parasitic inductances and drain resistance from S-parameters measured over frequency for one active bias condition. Given a value for the parasitic gate resistance R_g, all of the other equivalent-circuit parameters are uniquely extracted. The method is fast and robust, making it suitable for in-line statistical process tracking, as well as device modeling. A process tracking example for a 12-wafer 1864-device sample and FET modeling results up to 40 GHz are also presented.**

***Index Terms*—FET equivalent circuit, parameter extraction, semiconductor device modeling, small-signal model.**

I. Introduction

STATISTICAL process monitoring of GaAs FETs under high-volume production conditions requires a fast, consistent, and robust parameter-extraction method that can be performed in-line from a minimum number of measurements. Many techniques have been proposed for GaAs FET parameter extraction and these methods utilize optimization, extraction, or combined techniques. In optimization methods, the equivalent-circuit parameters are varied by some means to minimize an objective function [1], [2]. Optimization methods have been shown to work well, but typically require long computer run times [3]. Extraction methods take advantage of the fact that, for several variants of the FET equivalent-circuit model, the intrinsic element values can be uniquely determined from measured FET S-parameter data if the parasitic element values are known. The extraction problem is, therefore, reduced to accurately determining the parasitic element values that are typically deduced by measurement. The remaining equivalent-circuit parameters are then extracted directly from measured S-parameter data. Cold FET methods are often used to determine the parasitic elements, however, this technique requires FET S-parameter measurements at additional bias conditions [3]–[7]. Some methods combine extraction and optimization by varying only the parasitic element values and analytically extracting the remaining equivalent-circuit parameters [8]–[10]. Some notable work has been done on extracting parasitic element values from S-parameter data under active bias conditions. A technique for determining the parasitic inductances by comparing the modeled versus measured Z-parameters for the device was presented in [11]. It has also been shown that either the parasitic gate or source resistance can be extracted from the S-parameter data by satisfying constraints placed on the Y-parameters by the topology of the equivalent-circuit model [10], [12].

For the FET equivalent-circuit model to be consistent, the model parameters must be independent of frequency. This condition is exploited by some of the combined extraction methods to determine the parasitic element values. Shirakawa *et al.* [9] demonstrated that a particular value of parasitic gate inductance results in the extracted $C_{\rm gs}$ to be independent of frequency. This observation was applied to circuit element extraction by optimizing the parasitic elements with an objective of zero variance with respect to frequency for the extracted equivalent-circuit parameters.

In this paper, the consistency condition is applied to develop an analytic extraction method for the parasitic inductances and drain resistance. The method requires FET S-parameter measurements in the active region alone and is very fast, making it suitable for in-line process tracking. All equivalent-circuit parameters are extracted, except for the parasitic gate resistance R_g. The method may be used directly for parameter extraction if R_g is known or may be incorporated into the extraction loop of an optimization method.

II. Intrinsic Element and Source-Resistance Extraction

The assumed form of the FET equivalent-circuit model is shown in Fig. 1, where the intrinsic part of the model is within the dashed lines. Note that the controlling voltage for the current source is the total voltage across both $C_{\rm gs}$ and R_i, as in [13]. The intrinsic FET model is deembedded from the parasitic elements as follows:

$$\mathbf{Y}_{\rm Int} = \mathbf{Z}_{\rm Int}^{-1} = (\mathbf{Z}_{\rm FET} - \mathbf{Z}_{\rm para})^{-1} \tag{1}$$

where the Z-parameter matrix for the parasitic elements is

$$\mathbf{Z}_{\rm para} = \begin{bmatrix} R_g + R_s + j\omega(L_g + L_s) & R_s + j\omega L_s \\ R_s + j\omega L_s & R_d + R_s + j\omega(L_d + L_s) \end{bmatrix}. \tag{2}$$

Manuscript received April 19, 2000.

The authors are with TriQuint Semiconductor, Richardson, TX 75083-3938 USA.

Publisher Item Identifier S 0018-9480(01)05041-4.

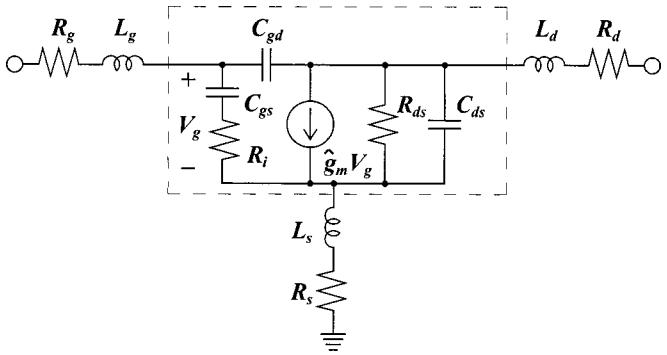

Fig. 1. FET equivalent-circuit model.

The Z-parameter matrix $\mathbf{Z}_{\rm FET}$ is converted from the measured S-parameter data for the transistor deembedded from the gate and drain feed networks. The Y-parameters of the intrinsic FET equivalent circuit are equal to

$$\mathbf{Y}_{\rm Int} = \begin{bmatrix} Y_{11}^{\rm Int} & Y_{12}^{\rm Int} \\ Y_{21}^{\rm Int} & Y_{22}^{\rm Int} \end{bmatrix} = \begin{bmatrix} j\omega C_{\rm gd} + \dfrac{j\omega C_{\rm gs}}{1+j\omega C_{\rm gs} R_i} & -j\omega C_{\rm gd} \\ -j\omega C_{\rm gd} + \hat{g}_m & \dfrac{1}{R_{\rm ds}} + j\omega(C_{\rm gd} + C_{\rm ds}) \end{bmatrix}. \tag{3}$$

The intrinsic equivalent-circuit element values are found by solving (3)

$$C_{\rm gd} = -\frac{\mathrm{Im}\{Y_{12}^{\rm Int}\}}{\omega} \tag{4}$$

$$C_{\rm ds} = \frac{\mathrm{Im}\{Y_{22}^{\rm Int}\} + \mathrm{Im}\{Y_{12}^{\rm Int}\}}{\omega} \tag{5}$$

$$R_{\rm ds} = \frac{1}{\mathrm{Re}\{Y_{22}^{\rm Int}\}} \tag{6}$$

$$\hat{g}_m = g_m e^{-j\omega\tau} = Y_{21}^{\rm Int} - Y_{12}^{\rm Int} \tag{7}$$

$$g_m = \sqrt{\left(\mathrm{Re}\{Y_{21}^{\rm Int}\}\right)^2 + \left(\mathrm{Im}\{Y_{21}^{\rm Int}\} - \mathrm{Im}\{Y_{12}^{\rm Int}\}\right)^2} \tag{8}$$

$$\tau = -\frac{1}{\omega}\tan^{-1}\left(\frac{\mathrm{Im}\{Y_{21}^{\rm Int}\} - \mathrm{Im}\{Y_{12}^{\rm Int}\}}{\mathrm{Re}\{Y_{21}^{\rm Int}\}}\right) \tag{9}$$

$$C_{\rm gs} = \frac{\beta\left(\mathrm{Im}\{Y_{11}^{\rm Int}\} + \mathrm{Im}\{Y_{12}^{\rm Int}\}\right)}{\omega} \tag{10}$$

$$R_i = \frac{\mathrm{Re}\{Y_{11}^{\rm Int}\}}{\beta\left(\mathrm{Im}\{Y_{11}^{\rm Int}\} + \mathrm{Im}\{Y_{12}^{\rm Int}\}\right)^2} \tag{11}$$

$$\beta = 1 + \left(\frac{\mathrm{Re}\{Y_{11}^{\rm Int}\}}{\mathrm{Im}\{Y_{11}^{\rm Int}\} + \mathrm{Im}\{Y_{12}^{\rm Int}\}}\right)^2. \tag{12}$$

For the assumed form of the equivalent-circuit model, note that

$$\mathrm{Re}\{Y_{12}^{\rm Int}\} = 0. \tag{13}$$

Since the main contributors to the real part of the feedback in a GaAs FET are the parasitic gate and source resistances, (13) has been used to extract additional information about these elements from the measured data. Sommer used (13) to extract ratios of the gate-to-source and drain-to-source resistances, reducing the parasitic element optimization space to five parameters [12]. Ooi *et al.* [10] used (13) to extract the parasitic gate resistance directly given values for the five other parasitic elements [10]. Results in some recently published literature suggest that it is very difficult to obtain consistent optimization results for the parasitic gate resistance. Kompa and Novotny recommend [14] that the gate resistance be determined by a cold FET method and be held constant during the optimization process. Niekerk and Meyer also studied this problem for a specific optimizer and determined that the gate resistance did not consistently converge to the correct value and better results were obtained if R_g was held fixed [1]. Considering these results, it was anticipated that it would be very difficult to extract the gate resistance consistently with (13). Therefore, for this study, (13) is solved for the source resistance given values for the other parasitic elements. Expanding (13) in terms of the source resistance

$$\mathrm{Re}\{Y_{12}^{\rm Int}\} = \mathrm{Re}\left\{\frac{-\left(\tilde{Z}_{12}^{\rm Int} - R_s\right)}{\left(\tilde{Z}_{11}^{\rm Int} - R_s\right)\left(\tilde{Z}_{22}^{\rm Int} - R_s\right) - \left(\tilde{Z}_{12}^{\rm Int} - R_s\right)\left(\tilde{Z}_{21}^{\rm Int} - R_s\right)}\right\} = 0 \tag{14}$$

where the intrinsic Z-parameter matrix is deembedded with R_s set equal to zero as follows:

$$\tilde{\mathbf{Z}}_{\rm Int} = \begin{bmatrix} \tilde{Z}_{11}^{\rm Int} & \tilde{Z}_{12}^{\rm Int} \\ \tilde{Z}_{21}^{\rm Int} & \tilde{Z}_{22}^{\rm Int} \end{bmatrix} = \mathbf{Z}_{\rm Int}\,|_{R_s=0}\,. \tag{15}$$

Equation (14) may be rearranged and solved with the quadratic equation. One of the roots produces a value for the source resistance too large to be physically meaningful and may be rejected. The physically meaningful solution for the source resistance is given in (16)–(20) as follows:

$$R_s = \frac{-B - \sqrt{B^2 - 4AC}}{2A} \tag{16}$$

$$A = -\mathrm{Re}\{\tilde{Z}_{11}^{\rm Int} + \tilde{Z}_{22}^{\rm Int} - \tilde{Z}_{12}^{\rm Int} - \tilde{Z}_{21}^{\rm Int}\} \tag{17}$$

$$B = -\mathrm{Re}\left\{\tilde{\Delta}^* + \tilde{Z}_{12}^{\rm Int}\left(\tilde{Z}_{11}^{\rm Int} + \tilde{Z}_{22}^{\rm Int} - \tilde{Z}_{21}^{\rm Int} - \tilde{Z}_{12}^{\rm Int}\right)^*\right\} \tag{18}$$

$$C = -\mathrm{Re}\{\tilde{\Delta}^* \tilde{Z}_{12}^{\rm Int}\} \tag{19}$$

$$\tilde{\Delta} = \tilde{Z}_{11}^{\rm Int}\tilde{Z}_{22}^{\rm Int} - \tilde{Z}_{12}^{\rm Int}\tilde{Z}_{21}^{\rm Int}. \tag{20}$$

Using (16), a value for the source resistance may be extracted at each measurement frequency that will satisfy (13).

III. Parasitic Inductance and Drain-Resistance Extraction

For the equivalent-circuit model shown in Fig. 1 to be consistent, the extracted intrinsic element values must be of constant

value, independent of frequency. However, if the parasitic element values are not correct, the extracted intrinsic elements will not be independent of frequency, as demonstrated in [9]. Shirakawa *et al.* [9] proposed a statistical method where the correct parasitic element values result in minimum variance with respect to frequency for the extracted equivalent-circuit elements. An extracted circuit element whose value is independent of frequency will also have zero slope with respect to frequency. A variant on the statistical method described in [9] is to determine a set of parasitic element values that result in zero slope with respect to frequency for the extracted equivalent-circuit elements. The extracted circuit element frequency slope parameters can be easily calculated with linear regression analysis as follows:

$$m_i = \frac{N\sum_{k=1}^{N} f_k i_k - \left(\sum_{k=1}^{N} f_k\right)\left(\sum_{k=1}^{N} i_k\right)}{N\sum_{k=1}^{N} f_k^2 - \left(\sum_{k=1}^{N} f_k\right)^2} \tag{21}$$

where N is the total number frequency points, f_k are the measurement frequencies, and i_k is the ith equivalent-circuit element value extracted at f_k. Using (21) and S-parameter data generated from the equivalent-circuit model, the sensitivity of the equivalent-circuit element slope parameters with respect to the parasitic elements were calculated as a functions of frequency. It was found that the parasitic element sensitivities of $R_{\rm ds}$, $C_{\rm gs}$, $C_{\rm gd}$, and g_m had the strongest frequency dependence. The equivalent-circuit elements R_i, τ, and $C_{\rm ds}$ had parasitic element sensitivities that were more independent of frequency. Changes in the parasitic elements will cause the extracted values for these parameters to shift by an approximately constant amount for all of the measurement frequencies. As expected, none of the equivalent-circuit element sensitivities with respect to R_g showed significant frequency dependence. Based on these observations, slope parameters for $R_{\rm ds}$, $C_{\rm gs}$, $C_{\rm gd}$, and g_m will be used to extract the parasitic inductances and drain resistance.

Assume that, for some initial guess for the parasitic elements, the application of (21) on the extracted element values produces nonzero slope parameters. This is expressed mathematically as

$$\mathbf{m}(\mathbf{p}) \neq 0 \tag{22}$$

where $\mathbf{m}(\mathbf{p})$ is a vector of slope parameters and is a function of the parasitic element vector $\mathbf{p}$ as follows:

$$\mathbf{m}(\mathbf{p}) = \left[m_{R_{\rm ds}}, m_{C_{\rm gs}}, m_{C_{\rm gd}}, m_{g_m}\right]^T \tag{23}$$

$$\mathbf{p} = [L_g, L_s, L_d, R_d]^T. \tag{24}$$

Now assume that some correction Δ can be added to $\mathbf{p}$ such that all of the slope parameters are equal to zero as follows:

$$\mathbf{m}(\mathbf{p}+\mathbf{\Delta}) = 0 \tag{25}$$

$$\mathbf{\Delta} = \left[\Delta_{L_g}, \Delta_{L_s}, \Delta_{L_d}, \Delta_{R_d}\right]^T. \tag{26}$$

The solution to (25) is the objective of this paper, and this equation may be solved with the damped Newton method [15]. The parasitic element vector is updated at each iteration with the following:

$$\mathbf{p}_n = \mathbf{p}_{n-1} + \lambda \mathbf{\Delta}_n \tag{27}$$

where λ is the damping factor. The nth correction vector is equal to

$$\mathbf{\Delta}_n = -\mathbf{J}(\mathbf{p}_{n-1})^{-1}\mathbf{m}(\mathbf{p}_{n-1}) \tag{28}$$

where $\mathbf{J}$ is the Jacobian matrix. The damping factor is used to improve the convergence of the method for cases were the initial guess is far from the correct solution. The damping factor may be set to a constant value or may be actively adjusted if the correction (28) does not decrease from one iteration to the next.

To proceed with the proposed iterative process, the Jacobian matrix must be populated. A Jacobian matrix element is equal to the partial derivative of the ith equivalent-circuit element slope parameter with respect to the jth parasitic element. Differentiating (21) with respect to the jth parasitic element

$$J_{ij} = \frac{\partial m_i}{\partial p_j} = \frac{N\sum_{k=1}^{N} f_k \frac{\partial i_k}{\partial p_j} - \left(\sum_{k=1}^{N} f_k\right)\left(\sum_{k=1}^{N} \frac{\partial i_k}{\partial p_j}\right)}{N\sum_{k=1}^{N} f_k^2 - \left(\sum_{k=1}^{N} f_k\right)^2}. \tag{29}$$

Partial derivatives of the ith equivalent-circuit elements are found by differentiating (4), (6), (8), and (10) with respect to parasitic elements

$$\frac{\partial R_{\rm ds}}{\partial p_j} = -R_{\rm ds}^2 \,{\rm Re}\left\{\frac{\partial Y_{22}^{\rm Int}}{\partial p_j}\right\} \tag{30}$$

$$\frac{\partial C_{\rm gs}}{\partial p_j} = \left(\frac{2-\beta}{\omega}\right)\left({\rm Im}\left\{\frac{\partial Y_{11}^{\rm Int}}{\partial p_j}\right\} + {\rm Im}\left\{\frac{\partial Y_{12}^{\rm Int}}{\partial p_j}\right\}\right) + \frac{2\sqrt{\beta-1}}{\omega}\,{\rm Re}\left\{\frac{\partial Y_{11}^{\rm Int}}{\partial p_j}\right\} \tag{31}$$

$$\frac{\partial C_{\rm gd}}{\partial p_j} = -\frac{1}{\omega}\,{\rm Im}\left\{\frac{\partial Y_{12}^{\rm Int}}{\partial p_j}\right\} \tag{32}$$

$$\frac{\partial g_m}{\partial p_j} = \frac{{\rm Re}\{Y_{21}^{\rm Int}\}}{g_m}\,{\rm Re}\left\{\frac{\partial Y_{21}^{\rm Int}}{\partial p_j}\right\} + \frac{{\rm Im}\{Y_{21}^{\rm Int}\} - {\rm Im}\{Y_{12}^{\rm Int}\}}{g_m} \cdot \left({\rm Im}\left\{\frac{\partial Y_{21}^{\rm Int}}{\partial p_j}\right\} - {\rm Im}\left\{\frac{\partial Y_{12}^{\rm Int}}{\partial p_j}\right\}\right). \tag{33}$$

Partial derivatives for the intrinsic Y-parameters are found by substituting (2) into (1) and differentiating with respect to the parasitic elements. Results of this calculation are as follows:

$$\frac{\partial \mathbf{Y}_{\rm Int}}{\partial L_g} = j\omega \begin{bmatrix} Y_{11}^{\rm Int}Y_{11}^{\rm Int} & Y_{11}^{\rm Int}Y_{12}^{\rm Int} \\ Y_{11}^{\rm Int}Y_{21}^{\rm Int} & Y_{12}^{\rm Int}Y_{21}^{\rm Int} \end{bmatrix} \tag{34}$$

$$\frac{\partial \mathbf{Y}_{\rm Int}}{\partial L_s} = j\omega \begin{bmatrix} Y_{11}^{\rm Int}\Sigma - 1/\Delta & Y_{12}^{\rm Int}\Sigma + 1/\Delta \\ Y_{21}^{\rm Int}\Sigma + 1/\Delta & Y_{22}^{\rm Int}\Sigma - 1/\Delta \end{bmatrix} \tag{35}$$

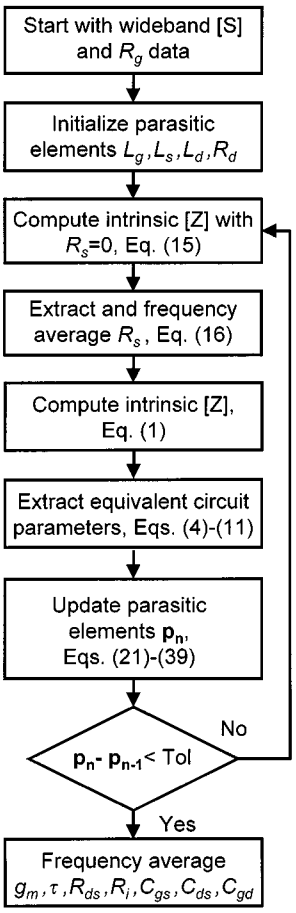

Fig. 2. Extraction algorithm.

$$\frac{\partial \mathbf{Y}_{\mathrm{Int}}}{\partial L_d} = j\omega \begin{bmatrix} Y_{12}^{\mathrm{Int}} Y_{21}^{\mathrm{Int}} & Y_{22}^{\mathrm{Int}} Y_{12}^{\mathrm{Int}} \\ Y_{22}^{\mathrm{Int}} Y_{21}^{\mathrm{Int}} & Y_{22}^{\mathrm{Int}} Y_{22}^{\mathrm{Int}} \end{bmatrix} \tag{36}$$

$$\frac{\partial \mathbf{Y}_{\mathrm{Int}}}{\partial R_d} = \begin{bmatrix} Y_{12}^{\mathrm{Int}} Y_{21}^{\mathrm{Int}} & Y_{22}^{\mathrm{Int}} Y_{12}^{\mathrm{Int}} \\ Y_{22}^{\mathrm{Int}} Y_{21}^{\mathrm{Int}} & Y_{22}^{\mathrm{Int}} Y_{22}^{\mathrm{Int}} \end{bmatrix} \tag{37}$$

$$\Delta = Z_{11}^{\mathrm{Int}} Z_{22}^{\mathrm{Int}} - Z_{12}^{\mathrm{Int}} Z_{21}^{\mathrm{Int}} \tag{38}$$

$$\Sigma = Y_{11}^{\mathrm{Int}} + Y_{22}^{\mathrm{Int}} + Y_{21}^{\mathrm{Int}} + Y_{12}^{\mathrm{Int}}. \tag{39}$$

A flowchart for the extraction algorithm is shown in Fig. 2.

IV. Results

The extraction method described above was implemented and tested on data for several devices. For the first example, extractions were performed on measured S-parameter data for a 300-μm gatewidth 0.25-μm gatelength millimeter-wave pseudomorphic high electron-mobility transistor (MMW pHEMT) device at a bias condition of $V\mathrm{ds} = 5.0$ V and $I\mathrm{ds} = 30$ mA. S-parameters were measured with a thru-reflect line (TRL) calibrated HP8510C using 2.4-mm ground–signal–ground (GSG) wafer probes. A damping factor of one and ten Newton iterations were used for the extraction. The method requires a value for the parasitic gate resistance R_g as an input. This value can be obtained by applying the cold FET technique. In our case, 0.25-μm MMW pHEMT is a production process and a large linear model database exists. Rather than applying the cold FET method to this specific device, a value for Rg was obtained by averaging the normalized gate resistances in the existing linear model database. The normalized average value for the gate resistance scaled to the device size under consideration is 0.5 Ω. The extracted values for the parasitic inductances and drain resistance as the iterations proceed are shown in Fig. 3. All four elements have converged after ten iterations and are within 10% of their final values after three iterations.

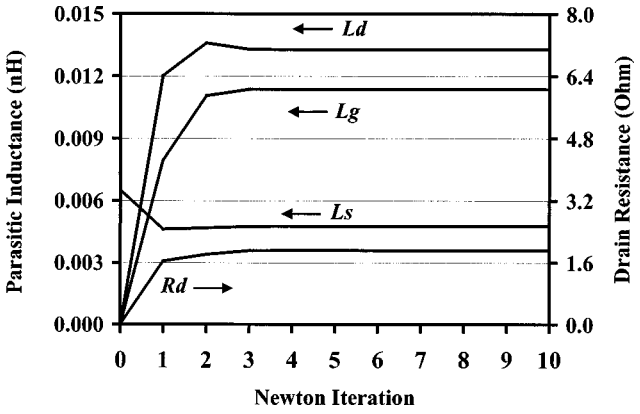

Fig. 3. Convergence of the parasitic elements.

The extracted equivalent-circuit element values are plotted in Fig. 4 as functions of frequency. As can be seen from Fig. 4, with the exception of measurement-induced ripple, elements R_{ds}, C_{gs}, C_{gd}, and g_m are approximately independent of frequency. The remaining circuit elements R_i, τ, R_s, and C_{ds} typically vary less than 10% from 10 to 40 GHz. To reduce the extraction data to a single value for each equivalent-circuit element, the data plotted in Fig. 4 was averaged over frequency from 5 to 40 GHz for R_{ds}, C_{gs}, C_{gd}, and g_m, and from 10 to 40 GHz for R_i, τ, R_s, and C_{ds}. The averaged element values listed in Table I were substituted into the equivalent circuit, and the modeled S-parameter data is compared to the measured results in Fig. 5. Over a frequency range of 2–40 GHz, the maximum observed magnitude error was at 2.1% and the worst-case phase error was -2.5°.

At low frequencies, measurement errors due to dynamic range limitations of the measurement system produce inaccurate results for some of the equivalent-circuit parameters. Similar difficulties were observed and noted in [12]. Using the values in Table I for the equivalent circuit, simulated intrinsic y-parameter data was generated for comparison to the measured results. Deviation between the measured and modeled data was observed at low frequencies for intrinsic $\mathrm{Re}\{y_{11}\}$, $\mathrm{Re}\{y_{12}\}$, $\mathrm{Im}\{y_{21}\}$, and $\mathrm{Im}\{y_{22}\}$. Error in these parameters produce the inaccurate low-frequency extractions for R_i, τ, R_s, and C_{ds}, shown in Fig. 4. The noted measurement errors do not significantly impact the extraction of C_{gs} because β was found to be approximately equal to unity at low frequencies. Similarly, since $\mathrm{Re}\{y_{21}\}$ is two orders of magnitude greater than $\mathrm{Im}\{y_{21}\}$, the measurement errors observed in $\mathrm{Im}\{y_{21}\}$ had little impact on the extraction of g_m. As illustrated in Fig. 5, using the extracted values for R_i, τ, R_s, and C_{ds} above 10 GHz produces good results over the entire measured frequency range.

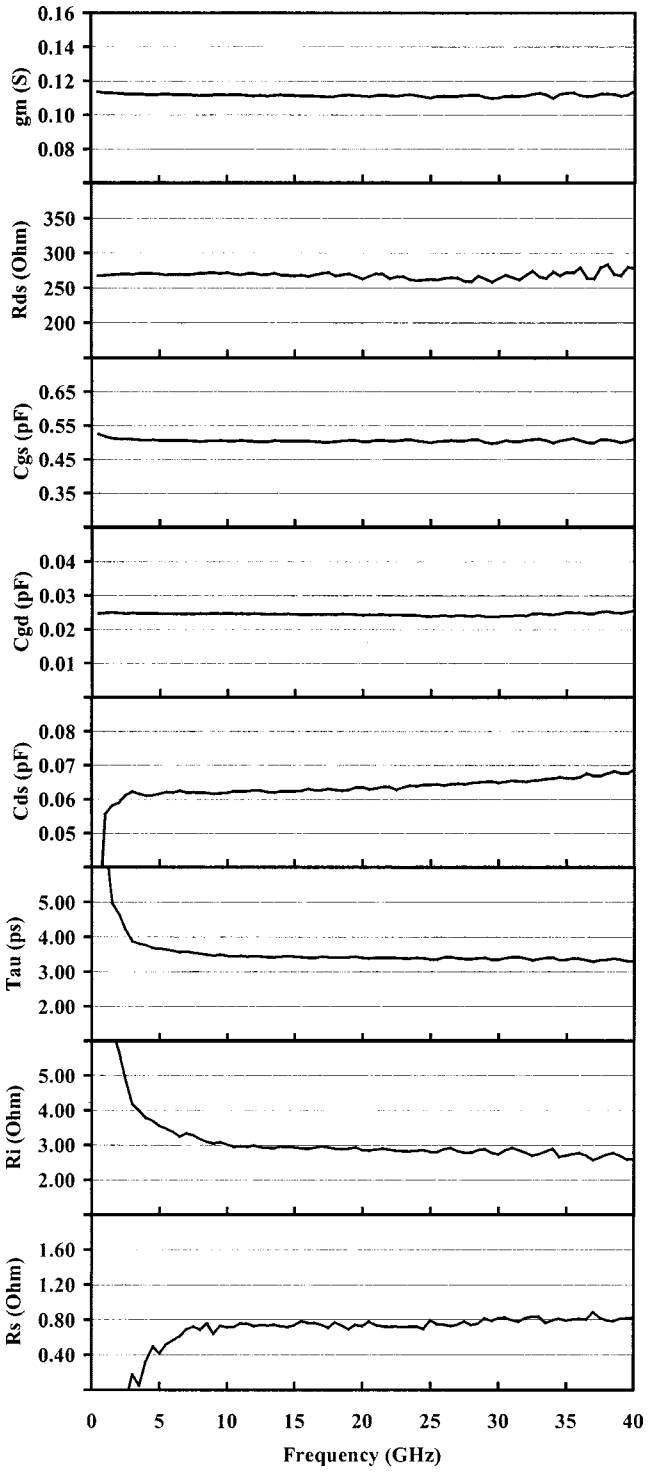

Fig. 4. Extracted equivalent-circuit elements.

The application for which this method was developed is in-line process tracking and wafer qualification. S-parameter data is taken with the automated on-wafer production RF-probe system for a standard FET coupon (SFC) at three standard bias conditions. The SFC is a GSG probable four-finger 300-μm gatewidth device grounded with two vias in the common source configuration. There are at minimum 15 SFCs per wafer, however, the number of SFCs varies from 15 to over 100 devices per wafer depending on the reticle layout. Wafers

TABLE I
EQUIVALENT-CIRCUIT PARAMETERS, 300-μm pHEMT AT $V\mathrm{ds} = 5$ V AND $I\mathrm{ds} = 30$ mA

Parameter	*Value*
g_m	0.1113 S
R_{ds}	267.8 Ω
C_{gs}	0.5041 pF
C_{gd}	0.0244 pF
C_{ds}	0.0662 pF
R_i	2.828 Ω
Tau	3.385 ps
L_g	0.0114 nH
L_d	0.0133 nH
L_s	0.0048 nH
R_g	0.5 Ω
R_d	1.915 Ω
R_s	0.760 Ω

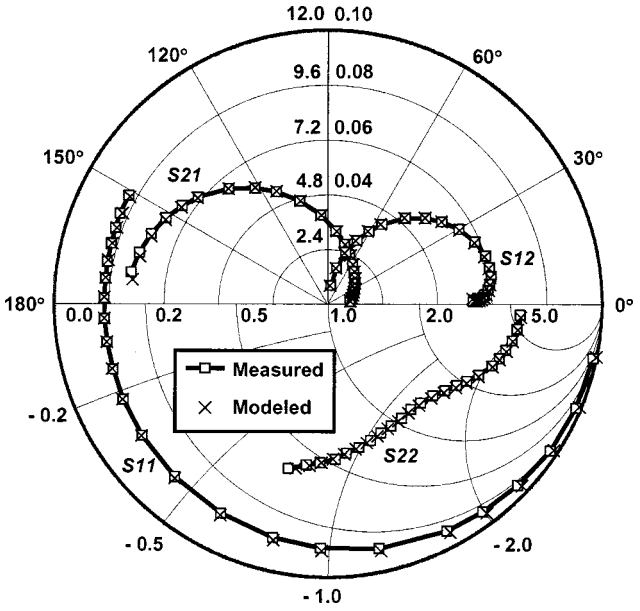

Fig. 5. Modeled versus measured S-parameters (0.5–40 GHz).

are qualified by comparing the extracted equivalent-circuit parameters to pass/fail limits for the process. The wafer data may also be compared to the long-term database to determine device performance relative to the process mean, and to help explain deviation from expected performance for the circuits processed on that wafer.

To demonstrate the application of this extraction technique to process tracking, SFC S-parameter data was analyzed from 12-MMW-pHEMT wafers (five lots). S-parameter data was taken for three bias conditions at 14 frequency points: 0.5 and 2 GHz to 26 GHz in 2-GHz steps. A gate resistance of 0.5 Ω was used for all of the extractions. Any process variation for R_g will, therefore, manifest itself as an additional variation in the other equivalent-circuit parameters. The execution time for ten Newton iterations with unity damping factor was 6 min and 28 s for 5592 model extractions (1864 devices at three bias conditions) on a SPARC 20 computer. Extraction results for g_m, C_{gs}, C_{gd}, and R_{ds} are shown in Figs. 6 and 7 for a bias condition of $V\mathrm{ds} = 3.0$ V and $I\mathrm{ds} = 15$ mA. Note that

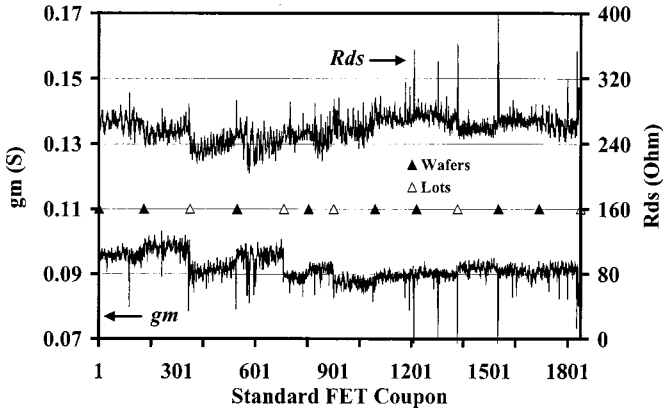

Fig. 6. Extracted g_m and $R_{\rm ds}$ for the SFC sample.

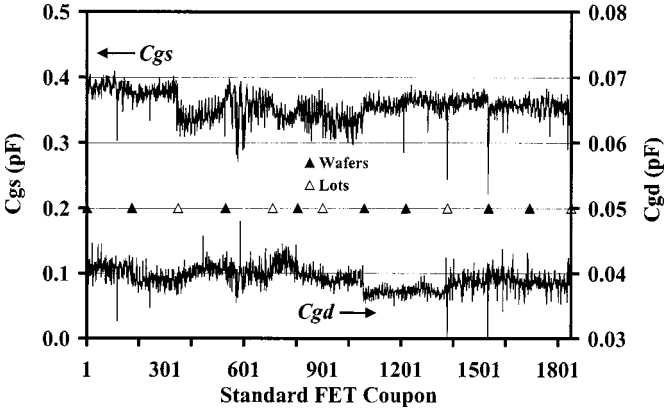

Fig. 7. Extracted $C_{\rm gs}$ and $C_{\rm gd}$ for the SFC sample.

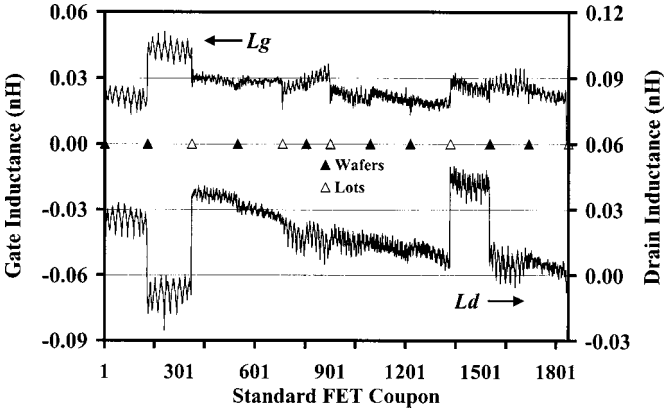

Fig. 8. Extracted gate and drain inductance for the SFC sample.

consistent results are typically observed over a wafer, however, some wafer-to-wafer variation is evident. The results shown in Figs. 6 and 7 have not been screened to any pass/fail limits, and nonoperational devices show up as spikes in the data. The extraction results for Lg, Ld, Rs, and Rd are shown in Figs. 8 and 9. Note the periodicity in the extracted parasitic elements for some of the wafers. The period corresponds to the rastering of the RF-probe chuck across the wafer. This suggests that there may be some stepping error from site to site. Also note the decrease in drain inductance and corresponding increase in gate inductance for the second wafer plotted in Fig. 8. This

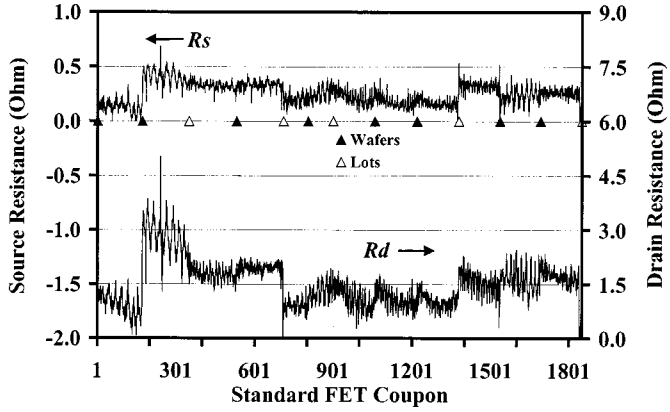

Fig. 9. Extracted source and drain resistance for the SFC sample.

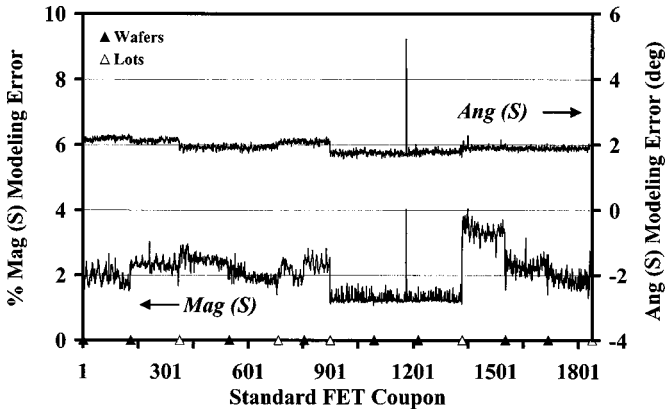

Fig. 10. Worst-case magnitude and phase modeling error for the SFC sample

suggests that the probes may have been shifted slightly toward the drain when the test was initially set up. Similarly, there is a increase in drain inductance with no corresponding decrease in gate inductance for the tenth wafer plotted in Fig. 8. A possible explanation would be an error in probe separation, where the probe on the gate side is nominally placed, but the drain side probe is shifted slightly away from the drain. The worse case observed S-parameter modeling errors for the SFC sample over the 0.5–26-GHz frequency range are plotted in Fig. 10. The maximum percentage magnitude error varied between 1%–4% with a mean of 2%. The maximum observed phase modeling error was typically 2°.

V. Conclusion

An analytic extraction method for the parasitic inductances, source resistance, and drain resistance has been described. The algorithm is fast and robust, making it suitable for in-line statistical process tracking, as well as device modeling. The method was applied to model a 300-μm pHEMT from 2 to 40 GHz, and worst-case S-parameter modeling errors of 2.1% and -2.5° were observed for magnitude and phase, respectively. A process-tracking example for an 1864 FET sample was also presented. The run time was approximately 0.07 s/extraction on a Sparc 20 computer, and the results demonstrate consistent equivalent-circuit element determination for a large sample of devices.

REFERENCES

[1] C. van Niekerk and P. Meyer, "Performance and limitations of decomposition-based parameter extraction procedures for FET small-signal models," *IEEE Trans. Microwave Theory Tech.*, vol. 46, pp. 1620–1627, Nov. 1998.

[2] H. Kondoh, "Accurate FET modeling from measured S-parameters," in *IEEE MTT-S Int. Microwave Symp. Dig.*, June 1986, pp. 377–380.

[3] C.-H. Kim, K.-S. Yoon, J.-W. Yank, J.-H. Lee, C.-S. Park, J.-J. Lee, and K.-E. Pyun, "A new extraction method to determine bias-dependent source series resistance in GaAs FETs," *IEEE Trans. Microwave Theory Tech.*, vol. 46, pp. 1242–1250, Sept. 1998.

[4] N. Rorsmann, M. Garcia, C. Karlsson, and H. Zirath, "Accurate small-signal modeling of HFET's for millimeter-wave applications," *IEEE Trans. Microwave Theory Tech.*, vol. 44, pp. 432–437, Mar. 1996.

[5] S. Yanagawa, H. Ishihara, and M. Ohtomo, "Analytical method for determining equivalent circuit parameters of GaAs FETs," *IEEE Trans. Microwave Theory Tech.*, vol. 44, pp. 1637–1641, Oct. 1996.

[6] M. Berroth and R. Bosch, "Broad-band determination of the FET small-signal equivalent circuit," *IEEE Trans. Microwave Theory Tech.*, vol. 38, pp. 891–895, July 1990.

[7] G. Dambrine, A. Cappy, F. Heliodore, and E. Playez, "A new method for determining the FET small-signal equivalent circuit," *IEEE Trans. Microwave Theory Tech.*, vol. 36, pp. 1151–1159, July 1988.

[8] F. Lin and G. Kompa, "FET model parameter extraction based on optimization with multiplane data-fitting and bidirectional search—A new concept," *IEEE Trans. Microwave Theory Tech.*, vol. 42, pp. 1114–1121, July 1994.

[9] K. Shirakawa, H. Oikawa, T. Shimura, Y. Kawasaki, Y. Ohashi, T. Saito, and Y. Daido, "An approach to determining an equivalent circuit for HEMTs," *IEEE Trans. Microwave Theory Tech.*, vol. 43, pp. 499–503, Mar. 1995.

[10] B.-L. Ooi, M.-S. Leong, and P.-S. Kooi, "A novel approach for determining the GaAs MESFET small-signal equivalent-circuit elements," *IEEE Trans. Microwave Theory Tech.*, vol. 45, pp. 2084–2088, Dec. 1997.

[11] E. Arnold, M. Golio, M. Miller, and B. Beckwith, "Direct extraction of GaAs MESFET intrinsic element and parasitic inductance values," in *IEEE MTT-S Int. Microwave Symp. Dig.*, June 1990, pp. 359–362.

[12] V. Sommer, "A new method to determine the source resistance of FET from measured S-parameters under active-bias conditions," *IEEE Trans. Microwave Theory Tech.*, vol. 43, pp. 504–510, Mar. 1995.

[13] W. Curtice and R. Camisa, "Self-consistent GaAs FET models for amplifier design and device diagnostics," *IEEE Trans. Microwave Theory Tech.*, vol. 32, pp. 1573–1578, Dec. 1984.

[14] G. Kompa and M. Novotny, "Highly consistent FET model parameter extractions based on broadband S-parameter measurements," in *IEEE MTT-S Int. Microwave Symp. Dig.*, June 1992, pp. 293–296.

[15] S. D. Conte and C. de-Boor, *Elementary Numerical Analysis—An Algorithmic Approach*. New York: McGraw-Hill, 1980.

Charles F. Campbell (S'85–M'87) was born in Evanston, IL, in 1965. He received the B.S.E.E., M.S.E.E., and Ph.D. degrees from Iowa State University, Ames, in 1988, 1991, and 1993, respectively.

From 1993 to 1998, he was with Texas Instruments Incorporated, Dallas, TX, where he was involved with monolithic-microwave integrated-circuit (MMIC) development and design. Since 1998, he has been with the Texas Division, TriQuint Semiconductor, Richardson, TX, where he is currently the Lead Engineer of the fiber-optic products business segment. His interests are compact high-power MMIC design techniques and device modeling.

Steven A. Brown (S'88–M'90) was born in New York, NY, in 1967. He received the B.S. degree in electrical engineering from Rensselaer Polytechnic Institute, Troy, NY, in 1988, and the M.S.E.E. from The University of Michigan at Ann Arbor, in 1990.

From 1990 to 1996, he served on active duty with the U.S. Air Force. In 1996, he joined Texas Instruments Incorporated, Dallas, TX, as a MMIC Designer. Since 1998, he has been with the Space Products Group, TriQuint Semiconductor, Richardson, TX. His interests include the development of high-power compact amplifiers for MMW applications.